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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/404,313	09/24/1999	TATSUHIKO AMAGAI	Q055935	8283

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EXAMINER	
HARPER, KEVIN C	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/404,313	AMAGAI ET AL.	
	Examiner	Art Unit	
	Kevin C. Harper	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments filed September 30, 2005 have been fully considered but they are not persuasive. Applicant argued that Yokoyama does not disclose a shared memory for writing and reading a header portion by a lower layer processing portion, where the header portion is used in a process of a higher layer processing portion. However, data stored in the memory (fig. 8, item 30) is used by the lower layer processor at packet reception and transmission (fig. 13, step 1034; fig. 12, item 1014-1016) and for processing by a higher level layer (fig. 14, step 1037-1038). However, a new rejection is given below in light of the newly cited Lo reference.

The indicated allowability of claims 16-24, 27-31 and 33-34 and the finality of the previous office action is withdrawn in view of the newly discovered reference(s) to Lo et al. (US 6,324,178). Rejections based on the newly cited reference(s) follow.

Claim Objections

Claim 30 is objected to because "IF" in the last line should be "IP". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 14-23 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6,324,178) in view of Yokoyama et al. (US 5,303,344) and Stoner et al. (US 6,052,383).

1. Regarding claim 14-23 and 25-29, Lo discloses a packet processing apparatus (fig. 4) for converting packet data through several layers (fig. 5, item 520 and 525; col. 8, lines 35-43). The apparatus comprises a packet memory for storing a user information portion of a packet data (abstract, lines 5-13; fig. 7, step 710). Further regarding claims 16-18, 21, 23, 27-29, the apparatus combines a new header portion with a user information portion stored in a packet memory as a packet to be transmitted (col. 9, lines 10-13 and 35-40). Regarding claims 17-20, 22-24, 26, 28-29, the lower layer portion is layer 2 and the higher layer portion is layer 3 (fig. 5, step 252; note: MAC at layer 2 and IP at layer 3 of an OSI reference model).

2. However, Lo does not disclose a shared memory. Yokoyama discloses a packet processing apparatus (fig. 8) comprising a shared memory (item 30) for storing in a same memory space part of each of the packet data accessed by several layers, including layer 2 and layer 3 processing (fig. 10; col. 6, line 61 through col. 7, line 2). A header portion (fig. 7) in the shared memory data is written at the time of packet reception and read at the time of packet transmission by a lower level layer (fig. 13, step 1034; fig. 12, item 1014-1016), and for processing by a higher level layer (fig. 14, step 1037-1038). The same memory space is accessed by the layer 2 and layer 3 processes (col. 7, lines 41-42; fig. 10; item E3; fig. 12, steps 1011-1012 and 1014; fig. 13, step 1034; fig. 14, step 1037). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a shared memory in the apparatus of Lo in order to provide a flexible protocol processor (Yokoyama, col. 1, lines 60-63).

3. Further, Lo in view of Yokoyama does not disclose that the layer 2 and layer 3 processing processors access the shared memory through separate buses or pipelined processing.

Stoner discloses separate component buses for pipeline processing (fig. 1, items 9, 11, 13 and 15). Further regarding claim 15, 20, 26 and 33, the shared memory (Figure 8, item 30) has multiple ports. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have the processors access the memory through different buses in the invention of Lo in view of Yokoyama in order to give dedicated access between the components (Stoner, col. 4, lines 11-14 and lines 43-54).

Claims 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6,324,178) in view of Yokoyama et al. (US 5,303,344) and Higuchi et al. (US 2003/0193965).

4. Regarding claim 30, Lo discloses a packet processing apparatus (fig. 4) for converting packet data through several layers (fig. 5, item 520 and 525; col. 8, lines 35-43). The apparatus comprises a packet memory for storing a user information portion of a packet data (abstract, lines 5-13; fig. 7, step 710). The apparatus combines a new header portion with a user information portion stored in a packet memory as a packet to be transmitted (col. 9, lines 10-13 and 35-40). The lower layer portion is layer 2 and the higher layer portion is layer 3 (fig. 5, step 252; note: MAC at layer 2 and IP at layer 3 of an OSI reference model).

5. However, Lo does not disclose a shared memory. Yokoyama discloses a packet processing apparatus (fig. 8) comprising a shared memory (item 30) for storing in a same memory space part of each of the packet data accessed by the layer 2 and layer 3 processing (fig. 10; col. 6, line 61 through col. 7, line 2). A header portion (fig. 7) in the shared memory data is written at the time of packet reception and read at the time of packet transmission by a lower level layer (fig. 13, step 1034; fig. 12, item 1014-1016), and for processing by a higher level layer (fig. 14, step 1037-1038). The same memory space is accessed by the layer 2 and layer 3

processes (col. 7, lines 41-42; fig. 10; item E3; fig. 12, steps 1011-1012 and 1014; fig. 13, step 1034; fig. 14, step 1037) and a layer 1 format packet is created (fig. 3, physical; fig. 2, item 40; fig. 8, item 22-4). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a shared memory in the apparatus of Lo in order to provide a flexible protocol processor (Yokoyama, col. 1, lines 60-63).

6. Further, Lo in view of Yokoyama does not disclose that the layer 2 process converting between IPv4 and IPv6. Higuchi discloses a layer 2 process (fig. 2, item 1006) for converting between IPv4 and IPv6. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a IPv4-IPv6 conversion in the invention of Lo in view of Yokoyama in order to provide a compatible IP packet to a network (Higuchi, para. 6, lines 1-11).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6,324,178) in view of Yokoyama et al. (US 5,303,344) and Higuchi et al. (US 2003/0193965) as applied to claim 30 above, and further in view of Tsuchiya et al. (US 6,118,784).

Regarding claim 31, the limitations of this claim have been addressed ion the rejection of claim 30 above, except that Lo in view of Yokoyama Higuchi does not disclose IP tunneling. Tsuchiya discloses IP tunneling (col. 2, lines 1-16). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have IP tunneling in the invention of Lo in view of Yokoyama and Higuchi in order to transmit an IP packet to a destination device (col. 2, lines 1-10).

Claims 24, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 6,324,178) in view of Yokoyama et al. (US 5,303,344) and Stoner et al. (US 6,052,383), as applied to claim 20 above, in further view of Albal et al. (US 4,821,265).

7. Regarding claims 24 and 32-34, these limitations have been addressed in the rejection of claim 20 above, except that Lo in view of Yokoyama and Stoner does not disclose storing an entire packet. Albal discloses a packet memory (Figures 1 and 2, item 19) for storing an entire packet at a communication interface. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a packet memory in the invention of Yokoyama in order to hold packets not ready for transmission from the interface (items 60, 62, 84 and 86; col. 7, lines 61-64).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Harper whose telephone number is 571-272-3166. The examiner can normally be reached weekdays from 11:00 AM to 7:00 PM ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao, can be reached at 571-272-3174. The centralized fax number for the Patent Office is 571-273-8300. For non-official communications, the examiner's personal fax number is 571-273-3166 and the examiner's e-mail address is kevin.harper@uspto.gov.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications associated with a customer number is available through Private PAIR only. For more information about the PAIR system, see portal.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin C. Harper

October 14, 2005

Seema S. Rao 10/17/05

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